REMARKS

This is a Response to the Office Action mailed March 27, 2006. Claims 2-27 are currently pending. Claims 2, 3, and 14 have been amended to correct antecedence errors.

Applicants thank the Examiner for the withdrawal of the previous prior art rejections in response to applicants' amendment.

The Examiner has rejected claims 2-27 under 35 U.S.C. § 103(a) as being unpatentable over admitted prior art and IBM Technical Disclosure Bulletin NN74091034: "Circuit Diagnosis and Design Analysis System" (hereafter *IBM Tech*).

Prior to addressing the rejection of the claims, some aspects of the disclosed embodiments of the invention will be discussed in comparison to the applied reference. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the subject matter described in the applied reference, do not define the scope or interpretation of any of the claims. Instead, such discussed differences are merely intended to help the Examiner appreciate important claim distinctions discussed thereafter.

Referring first to the Figure of the specification, an integrated memory device 1 is shown, which includes a control logic circuit portion 4, a memory array 2, and associated circuitry 3. According to an embodiment of the invention, an external test operation control device 9 can be coupled to the device 1 and the individual portions of the device 1 can be isolated and tested. For example, the specification states, beginning at line 21 of page 5, "[t]his not only allows the circuit portions of the device 1 to be controlled as desired, but also the control logic 4 itself to be isolated and tested for operability in a self-diagnosis mode." The specification also states, "the test operation control device 9 may also comprise logic circuitry to simulate the control logic 4, for the purpose of testing and observing the memory array 2 directly, and in isolation from the control logic" (page 5, lines 15-18). Thus, it can be seen that the disclosed embodiments are directed to methods and systems for testing individual circuits of *integrated devices*.

Attached as Appendix A is a copy of the three figures to which IBM Tech refers. IBM Tech is directed to a method of testing individual semiconductor chips of a circuit, in isolation from other components of the circuit, or for testing the other components of the circuit, with a single chip isolated from the circuit operation. For example, with reference to Figure 1, IBM Tech describes one system, beginning at about the sixth line of the text, in which a chip is isolated for testing of the overall circuit, and states, "The isolation gate of circuits being bypassed are activated to operate in the bypass mode, and the substituted circuits are appropriately programmed to provide the functions which substitute for the circuit of chip 20" (see lines 5-17). It can be seen from this text, as well as the remaining text of the reference, together with the figures, that IBM Tech offers no teaching or motivation to isolate a circuit of a single chip from other circuits on the same chip in order to independently test the isolated circuit, but teaches only the disabling of one or more entire chips to test either neighboring chips, or the overall circuit in the absence of the disabled chip.

Claim 2 recites (with emphasis added):

> A method of testing an electronic memory device that includes a control logic circuit portion, a matrix array of memory cells, and storage circuitry *integrated together on a semiconductor substrate*, the method comprising:
>
> loading test data and/or instructions into the control logic circuit portion using a test operation control device, temporarily, said test operation control device being external of, and temporarily connected to, said memory device, said test operation control device having a matrix cell array external to the memory device; and
>
> testing the logic circuit of the memory device by using the external matrix cell array to simulate the matrix array of memory cells of the memory device.

As the Examiner has acknowledged, the admitted prior art fails to teach or suggest a method that includes testing a logic circuit of a memory device by using an external matrix cell array to simulate a matrix array of memory cells of *the same* memory device. IBM Tech cannot remedy this deficiency, since it does not provide any teaching regarding simulating a portion of an integrated circuit to test another portion of *the same* integrated circuit. All of the teachings of IBM Tech are directed to testing of complete chips or circuits including complete chips. Clearly,

claim 2 is allowable over a combination of IBM Tech with the admitted prior art, together with dependent claims 4 and 5.

Claim 3 recites (with emphasis added):

> A method of testing an electronic memory device that includes a control logic circuit portion, a matrix array of memory cells, and storage circuitry *integrated together on a semiconductor substrate*, the method comprising:
>
> loading test data and/or instructions into the control logic circuit portion using a test operation control device, temporarily, said test operation control device being external of, and temporarily connected to, said memory device, said test operation control device having a control logic external to the memory device; and
>
> testing the matrix array of the memory device by simulating the control logic circuit of the memory device using the external control logic.

As the Examiner has acknowledged, the admitted prior art fails to teach or suggest a method that includes testing a matrix array of a memory device by using an external logic circuit to simulate a control logic circuit of *the same* memory device. IBM Tech cannot remedy this deficiency, since it does not provide any teaching regarding simulating a portion of an integrated circuit to test another portion of *the same* integrated circuit. All of the teachings of IBM Tech are directed to testing of complete chips or circuits including complete chips. Clearly, claim 3 is allowable over a combination of IBM Tech with the admitted prior art, together with dependent claims 23 and 24.

Claim 6 is reproduced herebelow:

> A control device for testing an electronic memory device formed on a semiconductor substrate, the memory device having a matrix array of memory cells and a control logic circuit portion associated with the memory cell array, as well as circuitry associated with said control logic, the control device comprising:
>
> a memory unit external of and detachably connectable to the memory device, the memory unit configured to simulate the memory cell array during testing of the control logic circuit portion of the memory device.

The admitted prior art fails to teach or suggest a memory unit configured to simulate the memory cell array of an electronic memory device having a matrix array of memory cells and a control logic circuit *formed together on a semiconductor substrate*, for testing of the

control logic circuit portion of the memory device. IBM Tech cannot remedy this deficiency, since it does not provide any teaching regarding simulating a portion of an integrated circuit to test another portion of *the same* integrated circuit. All of the teachings of IBM Tech are directed to testing of complete chips or circuits including complete chips. Accordingly, claim 6 is allowable over a combination of IBM Tech with the admitted prior art. Dependent claims 7 and 8 are also allowable.

Claim 9 recites:

> A device comprising:
>
> an internal memory array integrated onto a semiconductor substrate;
>
> a control logic circuit integrated onto the semiconductor substrate; and
>
> a test control device, external to the semiconductor substrate, having a circuit for simulating the internal memory array to permit testing of the control logic circuit in isolation from the internal memory array.

The Examiner has acknowledged that the admitted prior art does not teach or suggest an external test control device having a circuit for simulating an internal memory array of an integrated circuit to permit testing of a control logic circuit of the same integrated circuit, in isolation from the internal memory array. IBM Tech cannot remedy this deficiency, since it does not provide any teaching regarding simulating a portion of an integrated circuit to test another portion of the same integrated circuit. Accordingly, claim 9, together with dependent claims 10-13, is allowable over the cited art.

Claim 14 recites:

> A method for testing a memory device having a memory array and a control logic circuit integrated onto a semiconductor substrate, comprising:
>
> connecting an external circuit to the memory device;
>
> performing test operations with the memory array and the external connected circuit, using the external connected circuit to simulate the control logic circuit; and
>
> observing interactions between the memory array and the external connected circuit.

The admitted prior art fails to teach or suggest a method that includes performing test operations with a memory array using an external connected circuit to simulate a control logic circuit integrated with the memory array on a semiconductor substrate. IBM Tech cannot remedy this deficiency, since it does not provide any teaching regarding simulating a portion of an integrated circuit to test another portion of the same integrated circuit. Accordingly, claim 14 is allowable over the cited art.

Claim 15 recites:

> A method for testing a memory device having a control logic circuit and a memory array integrated onto a semiconductor substrate, comprising:
>
> connecting an external circuit to the memory device;
>
> performing test operations with the control logic circuit and the external connected circuit, using the external connected circuit to simulate the memory array; and
>
> observing interactions between the control logic circuit and the external connected circuit.

The admitted prior art fails to teach or suggest a method that includes performing test operations with a control logic circuit using an external connected circuit to simulate a memory array integrated with the control logic circuit on a semiconductor substrate. IBM Tech cannot remedy this deficiency, since it does not provide any teaching regarding simulating a portion of an integrated circuit to test another portion of the same integrated circuit. Accordingly, claim 15 is allowable over the cited art.

Claim 16 recites:

> A device, comprising:
>
> a semiconductor substrate;
>
> a memory array formed on the substrate;
>
> a control logic circuit formed on the substrate and configured to control operation of the memory array under normal operating conditions; and

> bypass circuitry formed on the substrate, and configured to permit substitution of an external memory array configured to simulate the memory array formed on the substrate, for the purpose of testing the control logic circuit separately from the memory array formed on the substrate.

The admitted prior art fails to teach or suggest a device comprising a memory array and a control logic circuit integrated on a substrate, and including bypass circuitry formed on the substrate and configured to permit substitution of an external memory array configured to simulate the memory array formed on the substrate. IBM Tech cannot remedy this deficiency, since it does not provide any teaching regarding any structure formed on a substrate for bypassing only a portion of the circuitry on the substrate, nor does not provide any teaching regarding simulating a portion of an integrated circuit to test another portion of the same integrated circuit. Accordingly, claim 16 is allowable over the cited art, together with dependent claims 17 and 18.

Claim 19 recites:

> An integrated semiconductor device configured to undergo testing by an external testing device, comprising:
>
> a non-volatile memory array;
>
> a control logic circuit configured to selectively program, read, and erase cells of the non-volatile memory array; and
>
> an instruction set configured to bypass the memory array, such that, when the instruction set is activated, the control logic circuit is configured to program, read, and erase cells of a memory array of the external device, in simulation of the non-volatile memory array.

The admitted prior art fails to teach or suggest an integrated semiconductor device comprising a memory array and a control logic circuit, and including an instruction set configured to bypass the memory array, such that, when the instruction set is activated, the control logic circuit is configured to program, read, and erase cells of a memory array of an external device. IBM Tech cannot remedy this deficiency, since it is also silent with regard to an instruction set configured to bypass a portion of an integrated circuit while enabling another portion of the same integrated circuit. Accordingly, claim 19 is allowable over the cited art, together with dependent claims 20 and 21.

Claim 22 recites:

> An integrated semiconductor device configured to undergo testing by an external testing device, comprising:
>
> a non-volatile memory array;
>
> a control logic circuit configured to selectively program, read, and erase cells of the non-volatile memory array; and
>
> an instruction set configured to bypass the control logic circuit, such that, when the instruction set is activated, the non-volatile memory array is configured to undergo program, read, and erase operations by a control logic of the external testing device, in simulation of the control logic circuit of the integrated semiconductor device. +27

The admitted prior art fails to teach or suggest an integrated semiconductor device comprising a memory array and a control logic circuit, and including an instruction set configured to bypass the control logic circuit, such that, when the instruction set is activated, the memory array is configured to undergo program, read, and erase operations by a control logic of an external testing device. IBM Tech cannot remedy this deficiency, since it is also silent with regard to an instruction set configured to bypass a portion of an integrated circuit while enabling another portion of the same integrated circuit. Accordingly, claim 22 is allowable over the cited art, together with dependent claim 27.

Conclusion

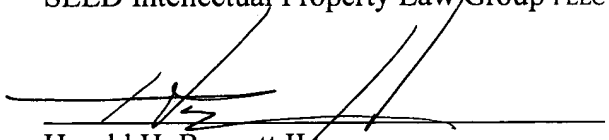
Overall, the cited references do not singly, or in any motivated combination, teach or suggest the claimed features of the embodiments recited in independent claims 2, 3, 6, 9, 14, 15, 16, 19, or 22, and thus such claims are allowable. Because the remaining claims depend from the allowable independent claims, and also because they include additional limitations, such claims are likewise allowable. If the undersigned representative has overlooked a relevant teaching in any of the references, the Examiner is requested to point out specifically where such teaching may be found.

In light of the above amendments and remarks, Applicants respectfully submit that all pending claims are allowable. Applicants, therefore, respectfully request that the Examiner reconsider this application and timely allow all pending claims. Examiner is encouraged to contact Mr. Bennett by telephone to discuss the above and any other distinctions between the claims and the applied references, if desired. If the Examiner notes any informalities in the claims, he is encouraged to contact Mr. Bennett by telephone to expediently correct such informalities.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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